High Performance SOI and Bulk CMOS 5GHz VCOs

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Abstract — **This paper presents a comparison of two 5GHz VCOs. One is implemented in an SOI process and the other in a conventional bulk CMOS process. The SOI design presents the lowest reported power (1.65mW, -110dBc/Hz@1MHz) in a 5GHz VCO, while the bulk device presents the lowest phase noise achieved in a 5GHz VCO (17.25mW, -126dBc/Hz@1MHz). The design tradeoffs are discussed.**

I. Introduction

Single chip 5GHz transceivers for the IEEE 802.11a WLAN and other markets require both low power and low phase noise VCOs. The phase noise has to be low enough to avoid compromising transmit Error Vector Magnitude (EVM) performance particularly at the high rate 54Mbps rate. Low power of course is important as usually WLAN NIC cards are plugged into laptop, tablet or PDA PCs that already have limited battery life.

This paper presents two designs on two different CMOS processes, one a 0.5um SOI process and one a generic 0.18um bulk process. It illustrates two ends of the performance/power spectrum. At one end the SOI design demonstrates extremely low power and moderate phase noise performance. At the other end, the bulk design demonstrates the lowest phase noise achieved in any monolithic 5GHz CMOS VCO.

II. CMOS VCO Noise Theory

Close-in phase noise of a CMOS VCO is mostly determined by 1/f or flicker noise upconverted to the oscillation frequency. Figure 1(a) shows the schematic of a typical CMOS VCO. It consists of an nMOS cross-coupled pair fed with a current source and tuned with an LC tank circuit. Part of the C is provided by source/drain-connected transistors used as varactors, which allow tuning control in a PLL.

There are numerous different flicker noise upconversion processes identified in the literature.

A. Common Mode Modulation to Frequency Modulation (CMM → FM)

The common mode (CM) here is referred to the DC level of the oscillator output. For an nMOS only topology, the reference node is the supply potential. When the CM is modulated by low frequency flicker noise in the current source tail transistor, the output waveform is shifted up or down and the average value over each period is no longer a constant. This upsets the average capacitance of the varactors, which assume a constant DC level. This modulation of the varactors results in an undesired modulation of the output frequency [1].

B. Amplitude Modulation to Frequency Modulation (AM → FM)

Flicker noise in the tail transistor can affect the oscillation frequency by modulating the current passing through the tuned circuit and cross-coupled transistors. When the bias current is modulated, the g_m of the differential pair changes and affects the oscillation amplitude. The varactors then transform it into FM [1]. This of more importance in current-limited VCOs than in hard-limiting voltage-limited VCOs.

C. Harmonic Distortion to Frequency Modulation (HD → FM)

The fundamental frequency of oscillation of an oscillator is affected by the harmonic content of its output waveform [2]. The deviation ($\Delta\omega$) is given as:

$$\frac{\Delta\omega}{\omega_{osc}} = \frac{1}{2Q^2}\sum_{n=2}^{\infty}\frac{n^2(1-n^2)}{(1-n^2)^2+n^2/Q^2}\cdot m_n^2 \qquad (1)$$

where n is the order of the harmonic, m_n is the normalized level of the n-th harmonic and Q is the Q of the tank [3]. The amount of harmonic content is closely related to the non-linearity in the g_m of the differential pair in the tank, which in turn is a function of the tail current. This is another means of flicker noise upconversion due to the tail transistor.

III. CMOS VCO Design Constraints

A. Topology

One can choose an nMOS only, pMOS only or complimentary topology for the differential pair. The

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nMOS only pair combines high g_m with immunity to noise upconversion process *A* mentioned in the previous section.

B. LC Tank Design

In general, phase noise can be minimized by increasing the signal energy in the tank while keeping the noise energy down. The total carrier energy stored in a tank is given by $\frac{1}{2}CV^2$, where V is the amplitude of the sinusoidal carrier signal and C is the total capacitance across the tank. Increasing C increases the total energy in the tank. For a constant frequency of operation, the total inductance in the tank, L, has to be lowered by the same factor, because the tank has to satisfy the following well-known equation:

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \quad (2)$$

A high L/C ratio implies the total energy stored in the tank is low and a low L/C ratio the opposite. This assumes constant tank Q and voltage swing. If we assume a fixed amount of noise power enters the tank through various routes, the obvious choice of L/C ratio for high noise immunity is to keep it low. However, this comes at a price where a low L/C ratio implies greater negative conductance ($-g_m$) to sustain oscillation amplitude, which in turn means higher power consumption.

C. Transistor sizing and oscillation amplitude

The cross-coupled pair can be biased in a number of different manners. Firstly, the transistors may be biased in continuous $-g_m$ mode where the transistors are kept in saturation throughout the oscillation cycle. This necessarily limits the oscillation amplitude. It can be shown that the amplitude is approximately $\frac{1}{2}V_{th}$, the threshold of the nMOS transistors used for the differential pair.

The transistors can also be biased in switch mode. This maximizes signal swing, hence increased SNR at the expense of taking the transistors out of saturation. This compromises the tank Q when they are not in saturation. Also, the noise upconversion process *C* discussed in the previous section becomes more significant.

It is not clear which regime yields the best results and so it is prudent (with research circuits) to allow for bias variation and transistor sizing such that both modes can be tested.

D. Single AC ground reference

The VCO circuit has two AC grounds, namely VDD and GND. In practice however, supply noise and the finite output impedance of the power supply leads us to desire one AC ground for the tank circuit. Since the common mode node is already defined by VDD due to the topology, VDD is chosen to be the AC ground reference for the tank circuit. Therefore, all the capacitors in the tank are connected to the VDD and the noise bypassing of the tank is also done with respect to VDD. However, as the tail current is defined by the V_{GS} of the tail transistor, the gate of the tail transistor is bypassed to GND. This does not interfere with tank noise bypassing to VDD, because there is high impedance between the tail transistor gate and the tank circuit. The single AC ground referencing of the tank is aimed towards improved supply rejection.

IV. VCO Designs

A. VCO1

VCO1 shown in Figure 1 is implemented in Peregrine Semiconductor's 0.5um UTSi (Ultra Thin Silicon) SOS (Silicon On Sapphire), single poly, 3 metal, and 14GHz f_T process. It was designed with an L/C ratio of 1.1nH/0.85pF = 1294. It has the following attributes:

- Continuous varactor tuning covers 200MHz (5.15GHz ~ 5.35GHz).
- VCO constant, K_v = 200MHz/V.
- Low power with decent phase noise performance was achievable owing to its high Q (~15) inductors. These are a consequence of very low substrate losses due to the SOI substrate.
- *SOI transistors do not suffer from body effect.* => V_{th} of the differential pair stays constant.
- Relatively High L/C ratio means high tank impedance. => little power is needed to overcome the loss and sustain oscillation.
- Die area, 0.760mm × 0.714mm = 0.543mm^2.

B. VCO2

The VCO in Figure 2 is implemented in a TSMC 0.18um Mixed-Mode, single poly, 6 metal, and 62GHz f_T process. The L/C ratio is 0.216nH/4.17pF = 52, which is quite low compared to previously reported designs. It has the following attributes:

- 8 steps of range tuning with 3-bit switched capacitor bank.
- Varactor tuning provides 20MHz of continuous tuning.
- VCO constant, K_v = 20MHz/V.
- Combined overall tuning range is 200MHz (5.13GHz ~ 5.33GHz).
- Inductor Q in a bulk process degrades quickly with number of turns and size of radius. Single turn

differential inductor used here has Q of around 15. High Q inductors in a standard bulk process are limited to small value inductors only.

- The differential pair transistors are placed in a deep-N-well and the well contacts are connected to the common source of the transistor pair.
  => no body effect for that transistor pair.
  Similarly, the varactor transistors are placed in a deep-N-well.
  => the back gate is at the same potential as the source/drain potential.
- Low L/C ratio means low tank impedance
  => need more power to overcome the loss and sustain oscillation.
- Die area, 0.702mm × 1.004mm = 0.705mm^2.

The microphotograph of each VCO is shown in Figure 1(b) and 2 (b) respectively.

V. RESULTS

Measuring close-in phase noise of a free running VCO directly with a spectrum analyzer is a difficult task, as the output frequency is unstable without a PLL. A phase noise measurement system, EUROTEST PN9000 utilizing a delay line acting as a frequency discriminator has been used in this work. This system reliably measures phase noise of a free running VCO up to 5MHz offset from the carrier.

Table 1 presents the results for the VCOs designed along with comparisons with recently published 5GHz VCO results.

Design	f_{osc} (GHz)	VDD (V)	I_{tail} (mA)	Power (mW)	Phase Noise*	FOM**
Ref [5]	4.00	2.5	7.5	18.75	-117	-176.3
Ref [4]	5.50	1.5	4.6	6.9	-116	-182.4
Ref [1] w/ tail	5.00	2.5	2	5	-110	-177.0
Ref [1] wo/ tail	5.00	2.5	2.9	7.25	-117	-182.4
VCO1	5.25	1.5	1.1	1.65	-110	-182.2
VCO2	5.33	1.5	11.5	17.25	-126	-188.2

*dBc/Hz @ 1MHz offset **dBc/Hz

Table 1. 5GHz VCO Comparison

VCO1 achieves a reduction in power compared to previous VCOs at some cost in phase noise. This oscillator would be useful in a less stringent application that was power sensitive (i.e. a mobile NIC card). VCO2 achieves the lowest phase noise in a 5GHz VCO reported to date at the expense of power consumption. This would be of use in a high performance application such as an WLAN access point or link radio where high power can be tolerated and high transmit powers require low transmit EVM. Figure 3 shows the SSB (single side band) phase noise for VCO1 while Figure 4 shows the SSB phase noise for VCO2. With VCO2, the corner between –30dB/decade slope and –20dB/decade slope is clearly visible between 200kHz and 300kHz offsets, whereas with VCO1, the corner is starting to appear after about 700kHz offset from the carrier. This suggests the 1/f noise corner frequency is somewhat lower with the VCO2 tail transistor than with the VCO1 tail transistor. There is a slight increase in phase noise up to 2dB with a none zero VCO constant in both cases, which is mostly due to the noise upconversion process *B* mentioned in section II.

The VCOs represent two corners in the design continuum of 5GHz VCOs. VCO1 maintains a relatively high L/C ratio in order to reduce the required g_m and in turn tail current to achieve a serviceable phase noise at very low power. VCO2 uses a low L/C ratio but correspondingly higher g_m and power consumption to achieve an extremely low phase noise at higher power. Together the oscillators may be used as reference points to design particular phase noise/power consumption. Table 1 also shows the representative figure of merit (FOM) for our VCOs and recently published examples. The figure of merit is defined as:

$$FOM = 10\log\left(\left(\frac{\Delta f}{f_{osc}}\right)^2 P_{DC}\right) + L(\Delta f) \qquad (3)$$

where $L(\Delta f)$ is SSB phase noise measured at Δf offset from the carrier f_{osc} (dBc/Hz) and P_{DC} is the DC power consumption in mW [6].

The table shows that VCO1 is competitive with its attendant low power consumption, while VCO2 has the best FOM of any 5GHz VCO published to date.

We have not made an attempt to compare the efficacy of SOI vs. bulk CMOS in this paper. That is the focus of ongoing work. It is interesting to note that the gate dimensions of the SOI technology are not aggressive and are rapidly being reduced. With optimization for low power and the better isolation of an SOI substrate, the SOI technology may well find application in very high performance radios (i.e. low power and high dynamic range).

VI. CONCLUSION

We have presented the design of two 5GHz VCOs that provide an illustration of the tradeoffs that may be made in VCO design with respect to power and phase noise. While not comparing SOI to bulk directly, we have shown that

competitive VCOs in terms of power or phase noise can be built in the respective technologies. VCO1 may be the basis of an extremely low power 5GHz transceiver, while VCO2 may be the basis of an extremely high performance single chip 5GHz transceiver.

ACKNOWLEDGEMENT

The support of Peregrine Semiconductor for fabrication and design support for VCO1 and Cisco Systems (Wireless Networking Business Unit) for fabrication and design support for VCO2 is acknowledged. Furthermore the support of Cadence Design Systems and Macquarie University in enabling the design of VCO1 is acknowledged. The authors would like to thank Jeffrey Harrison for helpful discussions.

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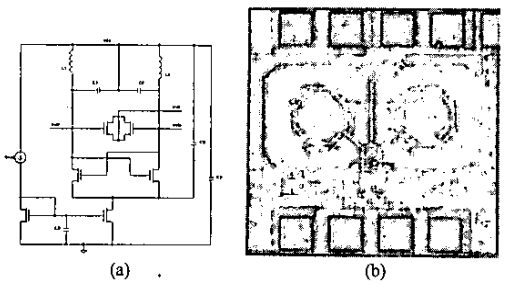
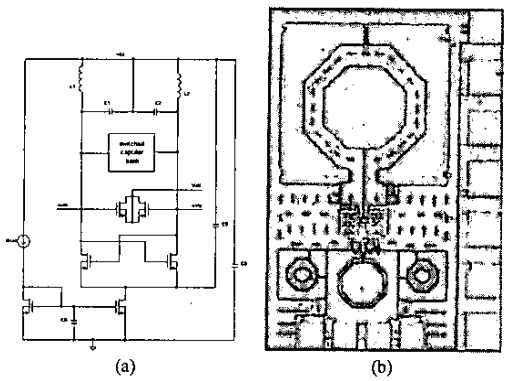


(a) (b)

Fig. 1. VCO1 (a) Schematic and (b) Microphotograph



(a) (b)

Fig. 2. VCO2 (a) Schematic and (b) Microphotograph

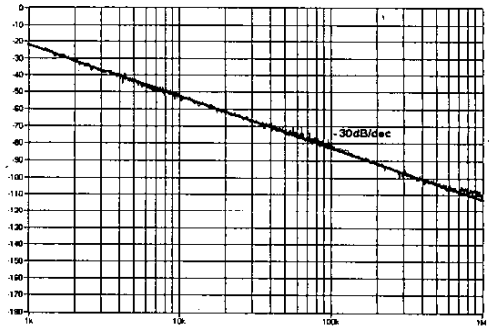


Fig. 3. VCO1 phase noise plot when K_V=200MHz/V

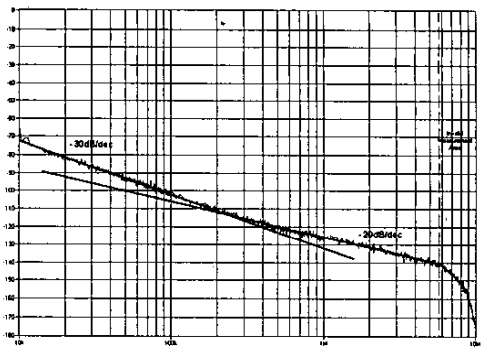


Fig. 4. VCO2 phase noise when K_V=20MHz/V